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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,899	06/29/2005	Motoo Asai	259189US90PCT	2986
22850	7590	06/23/2008		
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER JAHAN, BILKIS	
			ART UNIT 2814	PAPER NUMBER
			NOTIFICATION DATE 06/23/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/509,899	ASAI ET AL.	
	Examiner	Art Unit	
	BILKIS JAHAN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-71 is/are pending in the application.
- 4a) Of the above claim(s) 12-71 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>7/12/07, 6/29/07, 4/2/07, 2/14/07, 7/18/06, 7/12/06,</u> | 6) <input type="checkbox"/> Other: _____ |
| <u>6/21/06, 10/26/05, 10/12/05, 8/24/05, 12/17/04.</u> | |

DETAILED ACTION

The applicant's election with traverse claims 1-11 filed on April 24, 2008 has been acknowledged and not persuasive because the cited reasoning not found to be persuasive because MPEP 809.02(a) clearly defines that, "if the species *cannot be conveniently identified*, the claims may be grouped in accordance with the species to which they are restricted". Additionally, the applicant did not submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 6,-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi et al (US 2002/0127418 A1) in view of Kanber (5,312,765).

Regarding claim 1, Takeuchi et al disclose a substrate (Fig. 1) for mounting an IC chip comprising: a substrate 1 (Fig. 1, Para. 69, line 6) and, as serially built upon both faces (Fig. 1) thereof, a conductor circuit 90+10+11 (Fig. 1, Para. 74, line 10) and an interlaminar insulating layer 14+15 (Fig. 1, Para. 75, line 1) in an alternate fashion (Fig. 1) and in repetition (Fig. 1); a solder resist layer 12 (Fig. 1, Para. 75, line 10) formed as an outermost layer (Fig. 1); mounting an IC chip 18 (Fig. 1, Para. 76, line 2) but do not disclose an optical element mounted thereto, wherein an optical path for transmitting optical Signal is disposed so as to penetrate said substrate for mounting an IC chip.

- However, Kanber discloses an optical element 76 (Fig. 12, col. 6, lines 21-22) mounted thereto, wherein an optical path 92 (Fig. 12, col. 6, lines 38-41) for transmitting optical Signal (col. 6, lines 38-41) is disposed so as to penetrate said substrate 10 (Fig. 12, col. 4, line 54). Kanber teaches via inside the substrate is used to improve the heat dissipation efficiency and make strong substrate (col. 2, lines 38-41). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Takeuchi's substrate with Kanber's substrate to improve the heat dissipation efficiency and make strong substrate (col. 2, lines 38-41).

Regarding claim 2, Takeuchi et al modified by Kanber discloses said optical path for transmitting optical signal is constituted by a vacancy (Kanber, col. 6, lines 38-41).

Regarding claim 6, Takeuchi et al modified by Kanber do not disclose wherein a position at which said optical element is mounted is on a surface of the substrate for mounting an IC chip.

- Takeuchi et al modified by Kanber further disclose optical element is mounted is in the substrate 16 (Kanber, Fig. 12, col. 3, lines 49-50). However, the rearrangement of parts was held to have been obvious for a person having ordinary skill in the art. *In re japikse* 86 USPQ 70 (CCPA 1950) (see MPEP chapter 2100, section 2144.04, and page 136).

Regarding claim 7, Takeuchi et al modified by Kanber disclose said optical element is a light receiving element and/or a light emitting element (Kanber, col. 3, lines 49-50).

Regarding claim 8, Takeuchi et al further disclose an electronic component 18 (Fig. 1, Para. 76, line 2) is mounted on a surface of said substrate 1 (Fig. 1, Para. 69, line 6) for mounting an IC chip.

Regarding claim 10, Takeuchi et al modified by Kanber do not disclose a cross-sectional diameter of said optical path for transmitting optical signal is 100 to 500 nm.

- However, it would have been obvious to one of ordinary skill in the art to use any suitable diameter for the device, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to

discover the optimum or workable range by routine experimentation. See *In re Alner*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Claims 3, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Takeuchi et al* (US 2002/0127418 A1), *Kanber* (5,312,765) and further in view of *Lee et al* (5,452,283).

Regarding claim 3, *Takeuchi et al* modified by *Kanber* disclose limitations above but do not disclose said optical path for transmitting optical signal is constituted by a resin composition.

- However, *Lee et al* disclose said optical path for transmitting optical signal is constituted by a resin composition 76 (Fig. 6, col. 5, lines 27-30). *Lee* teaches resin in the optical path is used to align the optical path to the objective lenses of the disk array (col. 2, lines 43-46). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace *Takeuchi's* structure with *Lee's* structure including resin to align the optical path to the objective lenses of the disk array (col. 2, lines 43-46).

Regarding claim 9, *Takeuchi et al* modified by *Kanber* and *Lee et al* disclose a micro lens 30 (*Lee*, Fig. 7, col. 5, lines 53-58) is disposed on an end portion of said optical path for transmitting optical signal (*Lee*, Fig. 7).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi et al (US 2002/0127418 A1), Kanber (5,312,765) and further in view of Stone (5,530,288).

Regarding claim 4, Takeuchi et al modified by Kanber disclose limitations above but do not disclose said optical path for transmitting optical signal is constituted by a vacancy and a conductor layer around the vacancy.

- However, Stone discloses said optical path for transmitting optical signal is constituted by a vacancy and a conductor layer around the vacancy 29 (Fig. 2, col. 7, lines 45-50). Stone teaches conductive layer is used to connect from passive electronic components to the substrate and both sides of substrate component (col. 4, lines 63-67). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Takeuchi's structure with Stone's structure including conductive layer to connect from passive electronic components to the substrate and both sides of substrate components (col. 4, lines 63-67).

Claims 5, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi et al (US 2002/0127418 A1), Kanber (5,312,765) and further in view of Lee et al (5,452,283) and Stone (5,530,288).

Regarding claim 5, Takeuchi et al modified by Kanber, Lee, and Stone disclose all limitations in claims 1-4 above.

Regarding claim 11, Takeuchi et al modified by Kanber and Lee et al disclose all limitations in claims 1-10 as discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BILKIS JAHAN whose telephone number is (571)270-5022. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

BJ

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